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Efficient Power Management in DS-CDMA Reception: Introducing a Novel Analog Matched Filter Architecture

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Abstract: The Matched Filter (MF) stands out as the fastest method for gathering DS-CDMA signals, crucial in multimedia mobile terminal installations due to its power consumption implications. This paper introduces a novel analog matched filter architecture designed to mitigate power consumption and chip size concerns associated with the analog-to-digital (A/D) converter. Leveraging a sample-and-hold (S/H) circuit, the proposed filter executes correlation operations entirely in the analog domain, thereby reducing power consumption. Simulation results indicate that the suggested circuit consumes 2.3 mW at a 3.3 V supply for a 15-tap configuration with a chip rate of 16.7 MHz, demonstrating its potential to enhance mobile device performance.

1. Introduction

In modern mobile communication systems, achieving synchronization with the transmitter is essential for direct sequence code division multiple access (DS-CDMA) spread spectrum communication. Matching filters play a vital role in this process, undergoing extensive research to optimize their performance, especially in terms of high frequencies and low power consumption. Figures 1 and 2 provide visual representations of the DS-CDMA transmit portion and the actual transmitted signal, respectively. The transmitted signal undergoes modification through a combination of pseudo-random noise (PN) coding sequence and Phase Shift Keying (PSK). Matching filters facilitate the determination of the correlation function between the received signal and the PN Code, crucial for efficient demodulation and synchronization in DSCDMA systems.

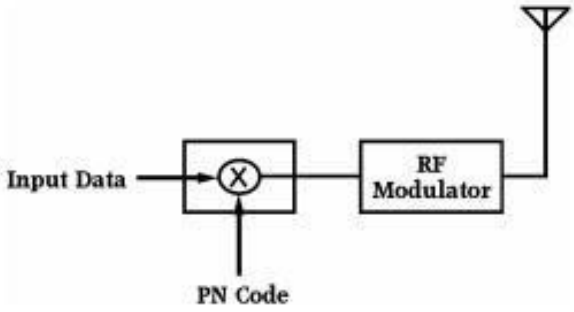

Figure 1. DS-CDMA system transmitter.

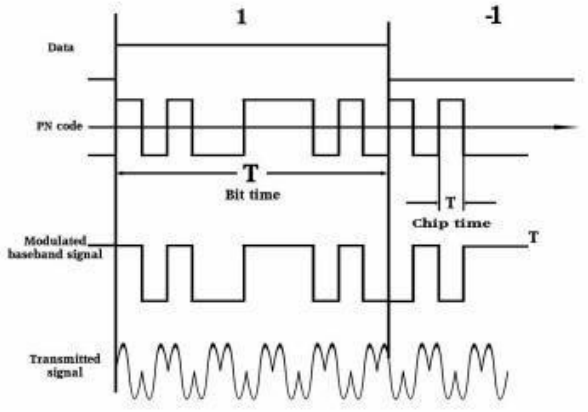

Figure 2. DS-spread spectrum modulation.

A matched filter is written as:

$$y(n) = \sum_{i=1}^{N} a_i x(n-i) \tag{1}$$

Where x(n) is the input signal, y(n) is the correlation output, and n is the number of taps (usually are 16 and 128), a_i is the PN code. a_i typically $\in \{-1, +1\}$, representing binary PSK (BPSK) demodulation.

Equation (1) signifies that correlation increases when the received signal aligns with the PN code at the receiver. This correlation peak serves as a crucial indicator for the receiver to detect and maintain synchronization necessary for information stream recognition and decoding. While Equation (1) can be computed using various methods, digital arithmetic is commonly employed. However, this paper introduces a pioneering approach—an analog matched filter utilizing a sample-and-hold (S/H) circuit. This circuit conducts correlation operations exclusively in the analog domain, eliminating the need for analog-to-digital conversion. Consequently, this innovation leads to reduced power consumption and chip space utilization.

2. Fundamental Architecture

a. Digital Matched Filter

Figure 3 illustrates the configuration of a typical digital matched filter, which initiates by converting the incoming analog signal into digital data using a robust high-speed A/D converter [6-8]. Subsequently, the digital data is sequentially transmitted to individual registers based on the PN code chip timing. The correlation value is then computed by summing the products of the digital data stored in register Dn and the PN code set in other registers. However, a key challenge associated with digital matched filters is the necessity for a high-performance A/D converter to minimize bit error rates. This requirement contributes to elevated power consumption and increased chip area, posing significant drawbacks.

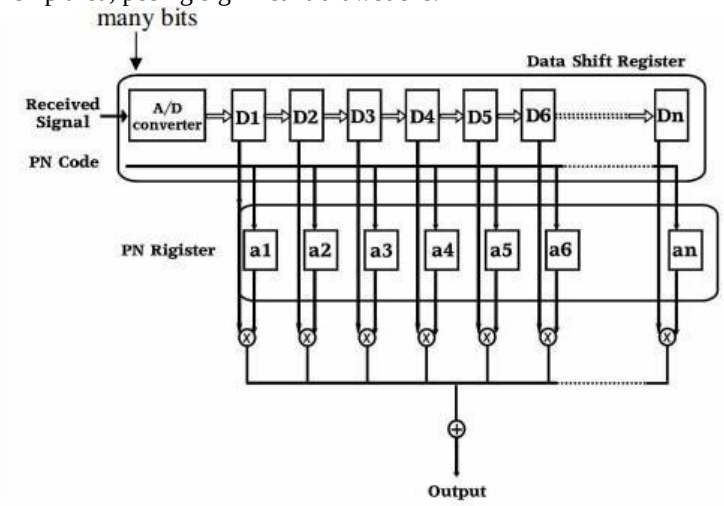

Figure 3. Conventional digital matched filter.

b. Analog Matched Filter

Diverging from the conventional digital matched filter approach, we present an innovative processing strategy depicted in Figure 4. Here, the received signal undergoes conversion to an analog value, and the data shift register incorporates a sample-and-hold (S/H) circuit. Analog circuitry governs the control panel. Notably, the proposed architecture necessitates only a signal line, obviating the need for an A/D converter. This streamlined design results in reduced chip area and power consumption, offering significant advantages over traditional methods.

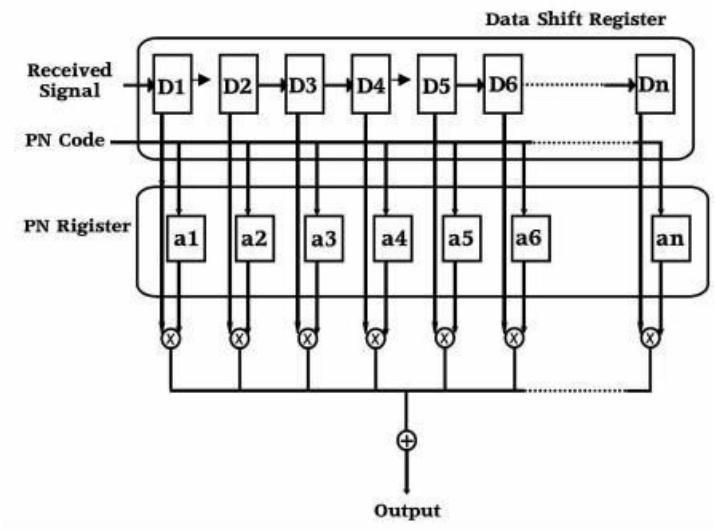

Figure 4. Proposed analog matched filter.

3. Proposed Circuit Design

Figures 5 and 6 provide visual representations of the essential components of the actual circuit and its corresponding timing diagram, respectively. In Figure 5, a clock-synchronized sample and-hold (S/H) circuit facilitates the sequential transfer of the input signal supplied to VIN to the subsequent stages. This synchronized operation ensures precise timing and orderly progression of the signal through the circuit, contributing to its efficient functioning.

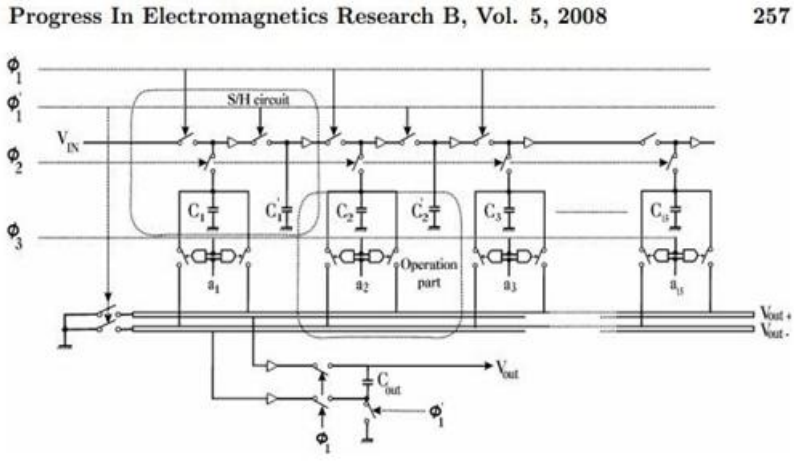

Figure 5. Operation circuit for proposed analog matched filter.

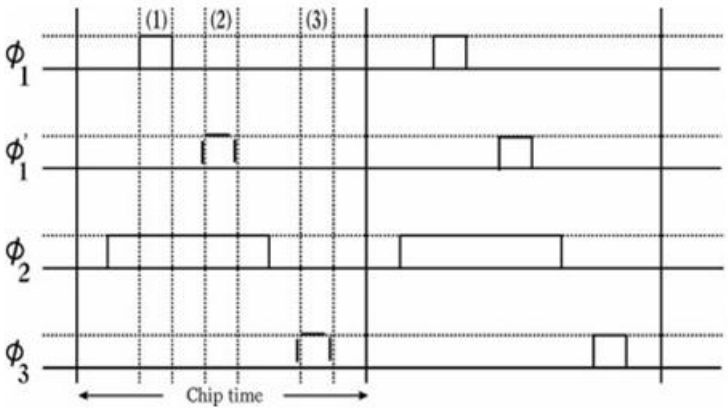

Figure 6 Switching sequence of the working circuit

The holding capacitors within the sample-and-hold (S/H) circuit retain the charges corresponding to the previous n-chip values of the received signal. Upon activation of switch Φ3, these charges are individually added based on the sign of the PN code. Subsequently, the resulting weighted charges, which are either positive or negative, are directed to the VOUT + and VOUT - nodes. Assuming an initial zero charge for each capacitor, Equation (2) emerges as a consequence of the exact conservation of charge [4]. Notably, equations (1) and (2) are interchangeable, highlighting their mutual relationship and significance in the circuit's operation.

$$V_{OUT}(n) = \sum_{i=1}^{N} \frac{C_i}{C_{TATAL}} V_{IN}(n-i) \tag{2}$$

This equation elucidates that the weight of each level can be adjusted based on the capacity of the sample-and-hold (S/H) circuit. In spread spectrum communication, weights of +1 or -1 are commonly employed, enabling the construction of all capacitors with uniform capacitance values. Here, 'A' equals 1 for weight +1 and 0 for weight -1. Following the execution of Equation (2), this circuit furnishes VOUT with the correlation value for each chip time. Figure 7 visually elucidates the operational principle of the proposed circuit, which is detailed as follows:

i. The voltage VIN of the input signal charges capacitor C_1. For data shifting, the charge held in the holding capacitor C_{n-1} is sampled and moved to the subsequent stage capacitor C_n.
ii. The signal from the subsequent destructive operation is preserved because C_n samples and retains the charge that it has stored.
iii. Depending on the sign of an, the charge stored in C_n is read out and placed into either the VOUT + or VOUT − nodes; VOUT + for an=1 and VOUT − for an=0.
iv. Following the earlier stages, correlation values are given as VOUT. The summing process and the holding signal are the two uses for the hold capacitor.

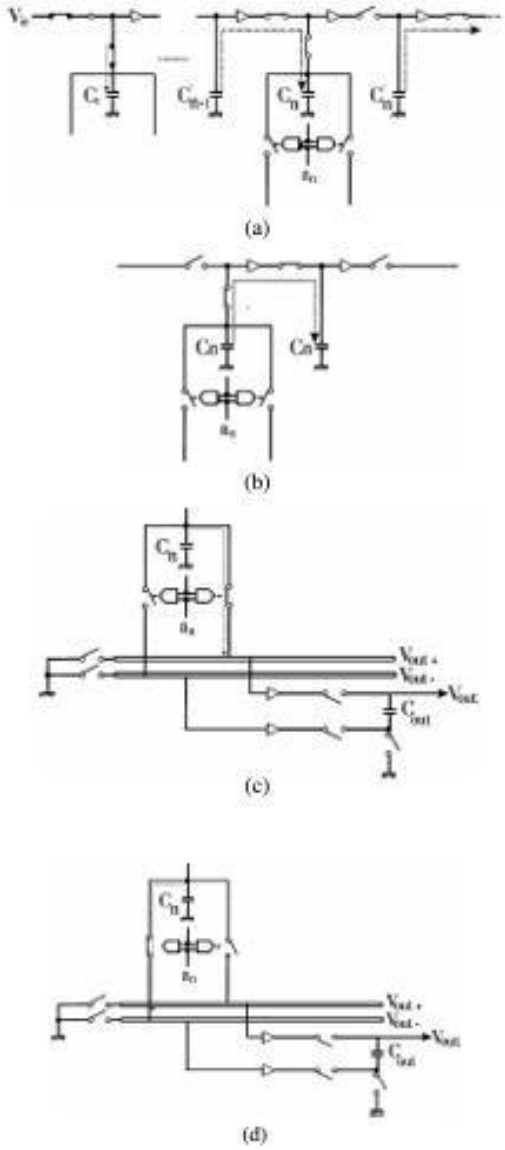

Figure 7. Principle of operation, (a) Interval (1), (b) Interval (2), (c) Interval (3) ($a_n = 1$), (d) Interval (3) ($a_n = 0$).

4. Design Considerations

a. Parasitic Effect

Considering the parasitic capacitances within the circuit provides insight into the operation of a circuit reading VOUT + and VOUT -. The schematic representation incorporating parasitic capacitance is depicted in Figure 8. The installation method of the capacitor significantly influences the value of parasitic capacitance [9]. The model includes polysilicon depletion capacitance, denoted by CJP, albeit its impact is minimal owing to capacitors' voltage coefficient falling within the range of 20 to 200 ppmV-1. Typically, there exists minimal parasitic capacitance on the top plate due to the capacitor connection, amounting to approximately 1/100 of Cn. Conversely, the circuit's junction capacitance predominantly contributes to the capacitance at the top plate node. It exhibits a high stress coefficient and encompasses roughly 20–30% of Cn. Additionally, the nonlinearities associated with source and drain junction capacitance in transistor switches introduce voltage dependence, expressed as CP = CP01 + VP Φ0.

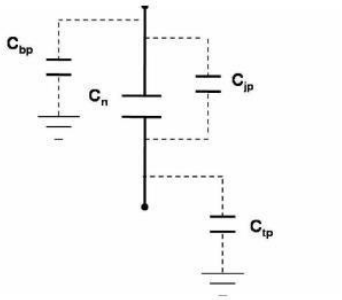

Figure 8. Sampling capacitor with parasitic capacitance shown.

Parasitic capacitance is also present at the bottom plate. Additionally, voltage dependency is characterized by Vjp. At VP = 0, the consumption is denoted as CP0. These capacitances possess the potential to introduce additional noise components into the correlation process, thereby potentially leading to errors in the sampling process [10–12]. Mitigating this impact can be achieved by reducing the switch size or increasing the sample capacitor size. As a consequence, the settling time constant (τ = Rswitch × [Cn + Cn]) escalates upon execution. In this scenario, there exists a trade-off between operational bandwidth and nonlinear error, as Rswitch represents the on-resistance of the hold mode switch. To ensure minimal switch charge injection error (0.3 μV), the sampling capacitor (Cn) and switch size (W/L) are meticulously chosen. **b.Noise**

In analog CMOS matching filters utilizing sample-and-hold (S/H) circuits, noise sources are present [13]. This noise primarily stems from input switch thermal noise, contributing to the sampled single sample noise power. Mathematically, this noise power is expressed as:

$$N_{thermal} = kT/ Cn$$

Where k = Boltzmann's constant and T is the temperature in Kelvin. This noise voltage 0.2 mV is very small compared to his code noise of other signals.

5. Simulation Results

The HSPICE simulation circuit proposed in this study was implemented using a 0.35 μm, 2poly, -3 metal, CMOS process. To ensure high voltage gain and high-frequency characteristics during simulation, a cascaded operational amplifier (op amp) configuration was employed. Moreover, each capacitor was meticulously sized to 0.2 pF. Assuming synchronization of the input signal illustrated in Figure 9 with the PN code, it can be inferred that the output peaks at that juncture. The output signal depicted in Figure 10 displays a peak every 15 chips, indicating that the proposed circuit effectively performs the requisite matched filter function. Additionally, Figure 11 presents a simulated instance of peak correlation derived from an analog signal modified post-capture. At every bit location in the data pattern, the code sequence under scrutiny undergoes testing. A perfect match and correlation peak manifest when every bit in the code sequence aligns with a corresponding pattern in the data.

The simulation results indicate that the matching filter effectively condenses most of the waveform's energy into a brief timeframe when the intended waveform is detected at the data input, which aids in recognizing signals. Table 1 summarizes the simulation findings, offering a clear overview of the filter's performance and its ability to process and identify signals.

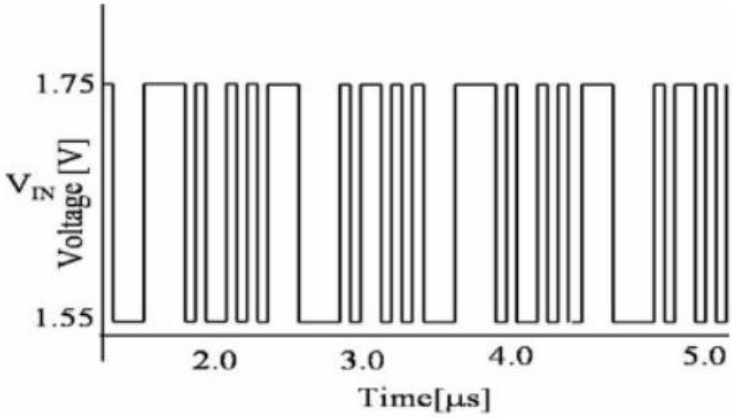

Figure 9. Input waveform.

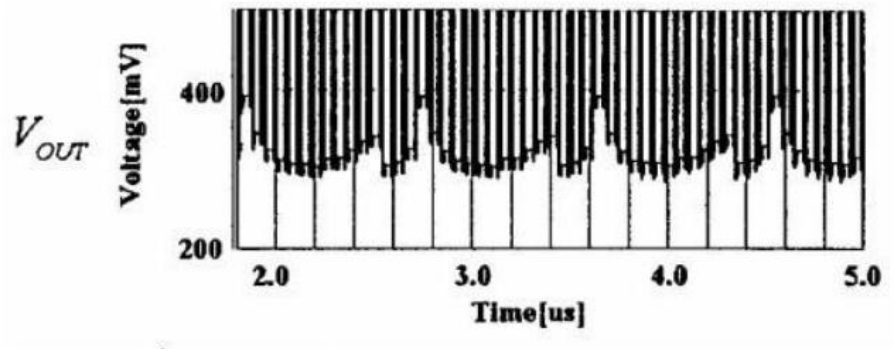

Figure 10. Output waveform.

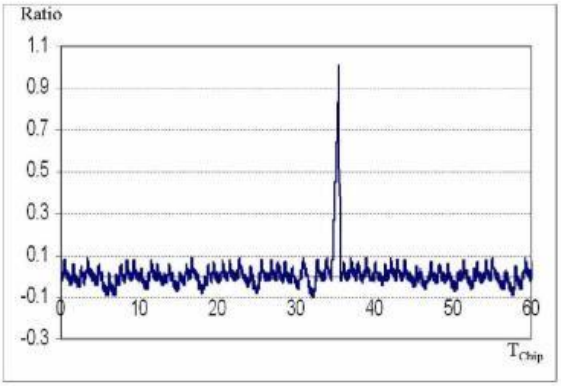

Figure 11. Example of correlation peak of analog matched filter

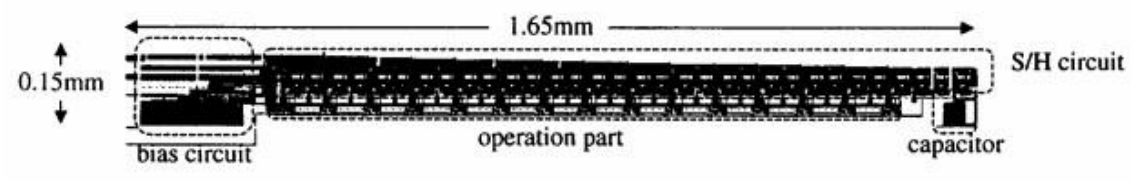

Figure 12. Analog matched filter layout

Using a 15-tap setup, the matched filter circuit achieves a chip rate of 16.7 MHz and consumes 2.3 mW of power with a 3.3 V supply. Figure 5 and Figure 12 depict the circuit configuration for the 15 taps, showcasing the design details. The chip occupies an area of 0.25 mm².

In Table 2, we compare the suggested circuit with existing analog matched filters and data from previous studies. When keeping the source voltage, frequency, and number of taps constant, we compute values in brackets for comparison. From the simulations, it's evident that our proposed circuit offers advantages in terms of size reduction and lower power consumption. Additionally, there's potential for further optimizing the power consumption of the cascaded amplifiers through careful adjustments.

Table 1. Simulation results.

Power supply voltage	3.3 V
PN code	Maximum length codes
The number of taps	15
Chip rate	16.7 MHz
Power consumption	2.3 mW

Table 2. Comparison with other reported matched filter circuits.

	Core area	Power	Power supply voltage	Techn -ology
Digital Architecture [5]	41.85 mm^2, 64 Tap (0.109 mm^2/Tap)	4 mW@2 MHz (0.21 μW/MHz·Tap·V^2)	5.0 V	1.2 μm
Analog Architecture [3]	85 mm^2, 128 Tap (0.664 mm^2/Tap)	225 mW@20 MHz (9.77 μW/MHz·Tap·V^2)	3.0 V	0.8 μm
Proposed Analog Matched Filter	0.25 mm^2, 15 Tap (0.017 mm^2/Tap)	2.3 mW@16.7 MHz (0.82 μW/MHz·Tap·V^2)	3.3 V	0.35 μm

6. Conclusion

The matched filter circuit, configured with 15 taps, achieves a chip rate of 16.7 MHz while operating on a 3.3 V supply and consuming 2.3 mW of power. Figure 5 illustrates the circuit layout for these 15 taps, while Figure 12 depicts the architecture of an analog matching filter. The chip area measures 0.25 mm².

In Table 2, we compare our suggested circuit with analog matched filters and other research findings. Assuming identical frequency, supply voltage, and number of taps, we calculate values in brackets for comparison. Our simulations indicate that the suggested circuit exhibits low power consumption and occupies a relatively small area. Moreover, there's potential to further reduce the power consumption of the cascaded amplifiers through careful adjustments.

7. References

[1]. Pickholtz, R. L., D. L. Schilling, and L. B. Milstein, "Theory of spread-spectrum communications — A tutorial," IEEE Transaction on Communications, Vol. 30, No. 5, 855– 884, May 1982.
[2]. Lee, W. C., "Overview of celluler CDMA," IEEE Transaction Vehicular Technology, Vol. 40, No. 2, 291–302, May 1991.
[3]. Chen, J., G. Shou, and C. Zhou, "High-speed low-power matched filter for W-CDMA: Algorithm and VLSI-architecture," IEICE Trans. Fundamentals, Vol. E83-A, No. 1, 75–81, January 2000.
[4]. Figueroa, M., D. Hsu, and C. Diorio, "A mixed-signal approach 264 Eltokhy and Mansour to high-performance low-power linear filters," IEEE J. Solid State Circuits, Vol. 36, No. 5, 264–270, May 2001.

[5]. Onodera, K. K. and P. R. Gray, "A 75-mW 128-MHz DS-CDMA base-band demodulator for high-speed wireless applications," IEEE J. Solid State Circuits, Vol. 33, No. 5, 753–761, May 1998.
[6]. Baier, A., "A low cost digital matched filter for arabitrary constant-envelope spread-spectrum wave-forms," IEEE Transaction on Communications, Vol. 32, 354–361, April 1984.
[7]. Kataoka, N., T. Kojima, M. Miyake, and T. Fujino, "Performance of soft decision digitqal matched filter in direct-sequence spread spectrum communication systems," IEICE Transaction, Vol. E74, 1115–1122, May 1991.
[8]. Wu, J., M. Liou, H. Ma, and T. Chiueh, "A 2.6 V, 44-MHz all digital QPSK digital-sequence spread spectrum transceiver IC," IEEE J. Solid-state Circuit, Vol. 32, 1499–1510, October 1997.
[9]. Slater, D. and J. Paulos, "Low volatge coefficient capacitors for VLSI processes," IEEE J. Solid State Circuits, Vol. 33, No. 5, 753–761, May 1998.
[10]. Sheu, B. and C. Hu, "Switched-induced error voltage on a switched capacitor," IEEE J. Solid State Circuits, Vol. SC-19, No. 4, 519–525, 1984.
[11]. Wegmann, G., E. Vittoz, and F. Rahali, "Charge injection in analog MOS switches," IEEE J. Solid State Circuits, Vol. SC-22, No. 6, 1091–1097, 1987.
[12]. Shyu, J. B., G. C. Temes, and F. Krummenacher, "Random errors effects in matched MOS capacitors and current sources," IEEE J. Solid State Circuits, Vol. SC-19, 948–955, 1984
[13]. Yoon, Y. C. and H. Leib, "Matched filtering in improper complex noise and applications to DS-CDMA," Conference Recordings PIMRC'95, 701–705, Toronto, Canada, Sept. 27–29, 1995