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Combination of Single Rail Encoding and Dual Rail Encoding In Register-Less Null Convention Logic

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Abstract: The concept of NULL convention logic (NCL) is introducing for constructing low-power robust asynchronous circuits. The presence of registers in conventional NCL can account up to 35 % overall power consumption. This brief presents the Combination of single rail and dual rail encoding in Register-less Null Convention Logic (RL-NCL) design paradigm, which achieves low power consumption by eliminating pipeline registers, simplifying the control circuit, and supporting fine-grain power gating to mitigate the leakage power of sleeping logic blocks. And also here introducing the concepts of single rail encoding and dual rail encoding. Data paths are composed of a mixture of dual-rail and single-rail domino gates. Dual-rail domino gates are limited to construct a stable critical data path. Based on this critical data path, the handshake circuits are greatly simplified, which offers the pipeline high throughput as well as low power consumption.

Index Terms: Fine grain power gating, Register-less Null Convention logic, Single rail and dual rail encoding.

I. Introduction

During the last decade, there has been a revival in research on asynchronous technology. Along with the continued CMOS technology scaling, VLSI systems become more and more complex. The physical design issues, such as global clock tree synthesis and top-level timing optimization, become serious problems. Even if technology scaling offers more integration possibilities, modularity and scalability are difficult to be realized at the physical level.

Asynchronous design is considered as a promising solution for dealing with these issues that relate to the global clock, because it uses local handshake instead of externally supplied global clock [2].
The attractive properties are listed as follows:

- low power consumption;
- high operating speed;
- no clock distribution and clock skew
- better composability and modularity;
- less emission of electromagnetic noise;

An asynchronous system comprises a set of autonomous functional modules, each of which communicates with others via handshaking only when it needs to send/receive data to/from its neighboring peers. Therefore, an asynchronous module is inherently data-driven and becomes active only when it needs to perform useful operations. Although an inactive asynchronous module consumes no dynamic power, it still suffers from static leakage power dissipation. Lately, a number of techniques have been proposed for utilizing fine grain power gating to diminish the static leakage power of asynchronous circuits [6]-[9],[13]-[15]. Especially, Multi-Threshold NCL (MTNCL) [6]-[9] is a variant of the conventional NCL paradigm that incorporates both multi-threshold CMOS (MTCMOS) and fine-grain power gating. In the MTNCL pipeline, a pipeline stage becomes active only when performing useful operations, and enters the sleep mode (i.e., being power-gated) when having no useful work to perform.

Both the conventional NCL and MTNCL paradigms require pipeline registers for separating two neighboring logic modules, in order to prevent a DATA/NULL token from overriding its preceding NULL/DATA token because of latency difference between pipeline stages. However, pipeline registers can account for up to 35% of overall power dissipation of the NCL/MTNCL circuit. This brief presents the register-less NCL (RL-NCL) design paradigm, which achieves low power by both eliminating the pipeline registers and supporting fine-grain power gating.

This paper presents a novel design method of asynchronous domino logic pipeline, which focuses on improving the circuit efficiency and making asynchronous domino logic pipeline design more practical for a wide range of applications. The novel design method combines the benefits of the four-phase dual-rail protocol and the four-phase bundled-data protocol, which achieves an area-efficient and ultralow-power asynchronous Register-less Null Convention Logic.

This reminder of this brief is organized as follows. In section II , introduce two related NCL design paradigms: conventional NCL and MTNCL. Section III describes the proposed Combination of dual rail encoding and single rail RL-NCL design paradigm. Section IV presents the simulation results. Section V concludes this brief.

II. Related Work

A. The Conventional NCL Paradigm

NCL is a self-timed logic paradigm in which control is inherent in each datum. NCL uses delay-insensitive code for data communication, alternating between set and reset phases. In the set phase, data changes from spacer (called NULL) to a proper codeword (called DATA); and in the reset phase it changes back to NULL. NCL combines DATA and NULL into a mixed path, usually represented by dual-rail or quad-rail signals. A dual-rail signal D consists of two wires, D^0 and D^1. D is logic 1 (DATA1) when $D^1 = 1$ and $D^0 = 0$; it is logic 0 (DATA0) when $D^0 = 1$ and $D^1 = 0$, and is NULL when both D^0 and D^1 are 0. NCL uses state-holding threshold gates with hysteresis [11]. An NCL gate is generally denoted as THmnW$w_1, \ldots, w_n$ where n is the number of inputs, m is the threshold of the gate, and $w_1, w_2, \ldots, w_n$ are the weights of inputs when they are greater than1. Assuming that the inputs are $x_1, \ldots, x_n$, then the output of an NCL gate is asserted when $x_1 w_1 + \cdots + x_n w_n d \geq m$ (see Table II for the set function of all the NCL gates). Since NCL gates have hysteresis, once the set function of a gate is satisfied and its output is asserted, it remains asserted until all its inputs are reasserted.

NCL circuits must be input-complete and observable in order to preserve delay-insensitivity. The input- completeness criterion states that outputs of a combinational circuit may not transition to DATA (NULL) before all the inputs have transitioned to DATA (NULL). However, according to the weak conditions of Seitz's delay-insensitive signalling, in circuits with multiple outputs, it is acceptable for some outputs to transition to DATA (NULL) without having a complete input DATA (NULL) set as long as all outputs cannot transition to DATA (NULL) before all inputs transition to DATA (NULL). Observability, on the other hand, requires that no orphans may propagate through a gate . An orphan is a signal transition on either a wire (wire orphan) or the output of a gate (gate orphan) that is not acknowledged by any primary output of a circuit. An output is said to acknowledge a signal transition if it always transitions following that signal transition. Wire orphans are not considered serious and can be ignored by assuming isochronic fork conditions, but gate orphans can cause delay sensitivity problems, and therefore must be avoided during circuit design.

B. Multi-threshold NCL Paradigm

As depicted in Fig. 1(a), in the Multi-Threshold NCL (MTNCL) pipeline, a pipeline stage, denoted by *Si*, comprises four components: a logic block *Li*, a data register *Ri*, a completion detector *CDi*, and an extra C-element (i.e., *TH22*).

In MTNCL, the logic blocks are built with MTCMOS threshold gates. Fig. 1(b) illustrates the structure of an MTCMOS threshold gate [7], which comprises two function blocks (i.e., 'hold-0' and 'set-to-1'), two high-V_T sleep transistors (Q1 and Q2) for power gating, and an output inverter with a pull-down transistor Q3.

An example of the MTCMOS threshold gate, *TH23*, is shown in Fig. 1(c).An MTCMOS threshold gate can operate either in the active mode (with control signal Sleep deasserted) or in the sleep mode (with control signal Sleep asserted). If the present input of logic block Li is DATA and sleepi is 0, transistors Q1 and Q2 in Fig. 1(b) are turned on, transistor Q3 is turned off, the MTCMOS threshold gates in Li begin to evaluate their outputs, and eventually the output of logic block L_i becomes DATA. If the present input of logic block Li is NULL and $Sleep_i$ is 1, transistors Q1 and Q2 in Fig. 1(b) are turned off, causing all MTCMOS threshold gates in Li to be power-gated, and transistor Q3 in Fig. 1(b) is turned on, forcing the outputs of all MTCMOS threshold gates in Li to become 0 (i.e., forcing the output of logic block Li to become NULL).

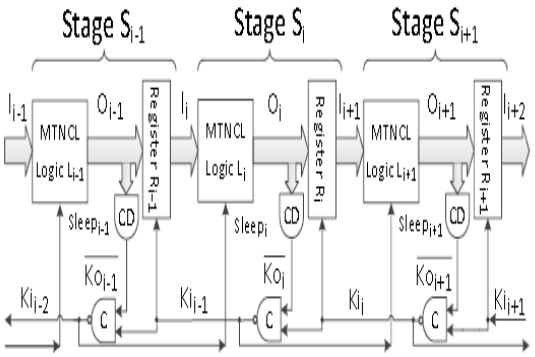

Fig 1(a) MTNCL Pipeline

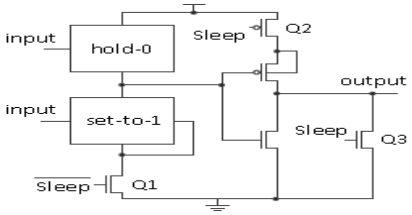

Fig 1(b) Structure of MTCMOS threshold gate

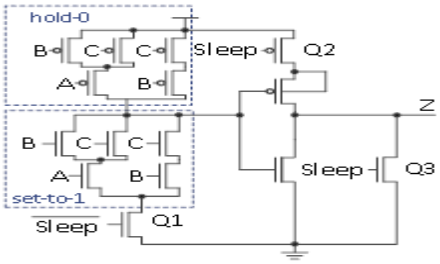

Fig 1(c) MTCMOS threshold gate TH_{23}

III. The Proposed Combination of Single Rail and Dual Rail Encoding in Register-Less Null Convention Logic

In this section, the proposed begin with the fine-grain power gating NCL (FPG-NCL) design paradigm, which supports fine-grain power gating, then derive the proposed combination of single rail encoding and dual rail encoding in register-less null convention logic, which achieves low power consumption by both supporting fine grain power gating and eliminating pipeline registers.

A) The FPG-NCL Paradigm

As depicted in Fig. 2, in the FPG-NCL paradigm, a pipeline stage, denoted by Si, comprises four components: 1) a logic block Li, which is built from MTCMOS threshold gates, 2) a data register Ri, 3) a completion detector CD_i, and 4) a C-element, which is used to control the operating mode (i.e., active or sleep) of logic block L_i. If Sleepi = 1/0, logic block L_i is in the active/sleep mode.

The data stream in FPG-NCL comprises a sequence of alternating DATA and NULL tokens, denoted by $D0$, $N0$, $D1$, $N1$, $D2$, $N2$, and so on, where Dk/Nk is the k-th DATA/NULL token. The operation of FPG-NCL is very similar to that of conventional NCL except that the logic blocks in FPG-NCL can be in the active or sleep mode.

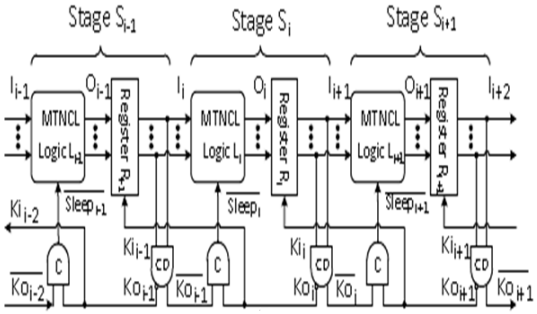

Fig 2 The FPG- NCL Pipeline

In FPG-NCL, logic block L_i enters the active mode when the following two conditions have both been fulfilled: 1) $Ko_i = 1$ (i.e., the preceding NULL token, N_{k-1}, has successfully passed through the input I_{i+1} of stage S_{i+1}), and 2) $\overline{Ko\ i-1}$= 1 (i.e., the next DATA token, denoted by Dk, has arrived at the input Ii of stage Si). Similarly, logic block Li enters the sleep mode when the following two conditions have both been fulfilled: 1) Ko_i =0 (i.e., the preceding DATA token, Dk, has successfully passed through the input I_{i+1} of stage S_{i+1}), and 2) $\overline{Koi-1}$=0(i.e, the next NULL token, denoted by Nk, has arrived at the input Ii of stage Si).

The purpose of using pipeline registers in FPG-NCL is to prevent a DATA token, denoted by Dk, from overriding its preceding NULL token Nk-1 as well as to prevent a NULL token, denoted by Nk, from overriding its preceding DATA token Dk. As an example, let us assume that 1) a DATA token Dk is now at Ii (see Fig. 3(a)), 2) its preceding NULL token N_{k-1} is at I_{i+1}, and 3) logic block Li is active. When Li finishes its evaluation and generates valid output, Dk advances to Oi. However, pipeline register Ri cannot latch Dk (i.e., the valid output of Li) until N_{k-1} has successfully arrived at I_{i+2}, which event causes Ko $_{i+1}$ (i.e., Kii) to become 1 and enables Ri to latch Dk. Therefore, pipeline registers in FPG-NCL can prevent a DATA/NULL token Dk/Nk from overriding its preceding NULL/DATA token Nk-1/Dk.

B. The Combination of dual rail encoding and single rail encoding RL-NCL Paradigm

The proposed RL-NCL requires no pipeline registers and is able to support fine-grain power gating. Fig. 3 shows the structure of the RL-NCL pipeline.

RL-NCL differs from FPG-NCL as follows:

1) RL-NCL requires no pipeline registers.

2) In the RL-NCL pipeline, Ko_{i+1}, instead of Ko_i (as in the case of FPG-NCL), is used as one input of the C-element generating signal $Sleep_i$. Namely, in RL-NCL, logic block L_i in stage S_i cannot begin evaluation/nullification for generating DATA/NULL token Dk/Nk at I_{i+1} until the preceding NULL/DATA token Nk-1/Dk has safely arrived at the input I_{i+2} of stage S_{i+2}. This restriction prevents a DATA/NULL token Dk/Nk from overriding its preceding NULL/DATA token Nk-1/Dk.

3) In RL-NCL, it is not viable for an input bit of the logic block to be directly wired to an output bit without MTCMOS threshold gates placed between them, because pure wires themselves cannot operate in the sleep mode. If a logic block does contain pure wires in its input-output network (e.g., stage Si)signals $Z1^0$and $Z1^1$ of logic block Li in Fig. 3(b)), every pure wire must be replaced with an MTNCL buffer.

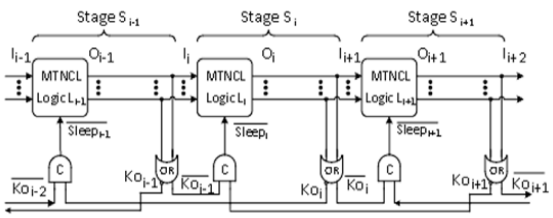

Fig 3 The proposed Combination of single rail and dual rail encoding in RL-NCL

4) In the RL-NCL pipeline, all MTCMOS threshold gates of a logic block begin evaluation/nullification at the same time, so the output bit on the critical path of the logic block becomes DATA/NULL after all the other output bits have already become DATA/NULL. Therefore, RL-NCL can employ an OR gate, whose two inputs are connected to the pair of wires associated with the output bit on the critical path of the logic block, to replace the completion detector for detecting whether the output of a logic block is DATA or NULL.

And also this paper presents a high-throughput and ultralow-power asynchronous domino logic pipeline design method, targeting to latch-free and extremely fine-grain or gate-level design. The data paths are composed of a mixture of dual-rail and single-rail domino gates. Dual-rail domino gates are limited to construct a stable critical data path. Based on this critical data path, the handshake circuits are greatly simplified, which offers the pipeline high throughput as well as low power consumption.

IV. Simulation Result

In order to evaluate the effectiveness of the proposed Combination dual rail encoding and single encoding RL-NCL, I have employed Three NCL paradigm- FPG NCL, RL NCL and Combination of single rail and dual rail RL-NCL, VHDL language is used for the design of this parallel counters. Modelsim 6.3f is used as the simulating tool. Xilinx ISE 8.1 is used as the synthesis tool. Experimental results include the simulation result of 8 bit kogge stone adder implemented as fine-grain power gating NCL, RL-NCL, Combination of single rail and dual rail encoding used in RL-NCL and the comparison of various parameters.

The 8 bit kogge stone adder is implemented in FPG-NCL. The adder has two input which we want to add, represented in dual rail encoding. And three other input one is carry input, other two are enabling signals. When carry input is zero and other enabling inputs are 1 then adder adds the inputs.

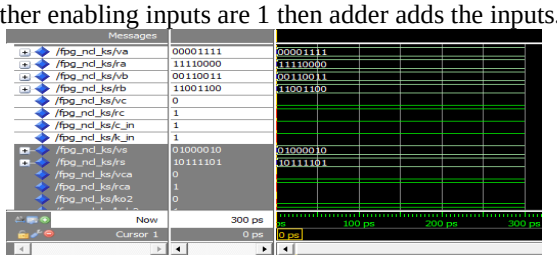

Fig 4(a) Wave form of 8 bit kogge stone adder impleneted as FPG-NCL

The RL-NCL implementation of an eight bit five stage pipelined kogge-stone adder which achieves low power consumption by eliminating pipeline registers, simplifying the control circuits, and supporting fine-grain power gating to mitigate the leakage power of sleeping blocks.

The adder has two input which we want to add, represented in dual rail encoding. And three other input one is carry input, other two are enabling signals. When carry input is zero and other enabling inputs are 1 then adder adds the input and gives the output.

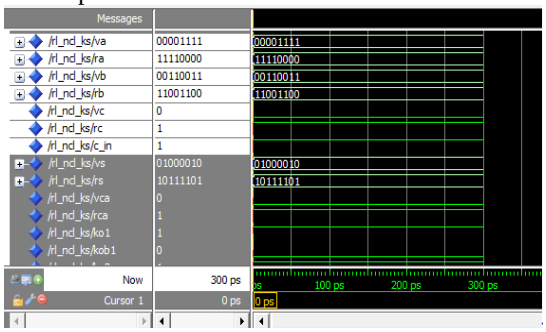

Fig 4(b) Wave form of 8 bit kogge stone adder implemented as RL-NCL

Combining dual rail encoding and single rail encoding in RL-NCL , it reduces more power consumption. Here main difference is the 7 bit input represented in single rail encoding and rest of the one input represented in dual rail encoding.

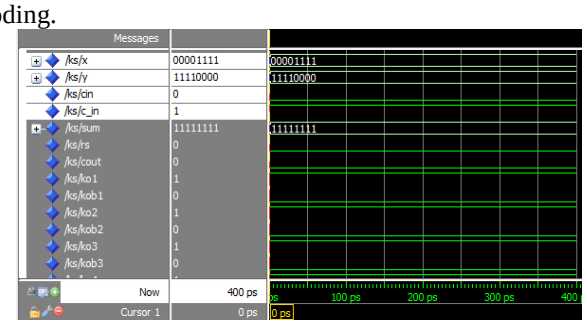

Fig 4(c) Wave form of 8 bit kogge stone adder impleneted as RL-NCL with combining single rail encoding and dual rail encoding

Table I gives a power dissipation comparison of the three NCL design paradigm FPG-NCL,RL-NCL, Combination of single rail and dual rail encoding in RL-NCL implementing the pipelined kogge stone adder with input data ranging from 10MHz to 900MHz. The power dissipation comparison of the three NCL paradigms, FPG-NCL, RL-NCL, Combination of single rail and dual rail encoding in RL-NCL , the FPG includes 200mW and it reduces to 188mW and our proposed system reduces to 50% of FPG-NCLThe advantage of low power dissipation in the RL-NCL paradigm comes from 1) eliminating pipeline registers, 2) replacing complex completion detectors with simpler OR gates, and 3) mitigating the leakage power of sleeping blocks by fine-grain power gating.

Table 1 Comparison table of path delay, power consumption and area of FPG-NCL, RL-NCL, Combination of single rail and dual rail encoding

	Path delay	Power consum ption	Area
FPG-NCL	38.162ns	200	1682
RL-NCL	32.200ns	188	1491
Combination of single rail an dual rail encoding	19.043ns	100	243

V. Conclusion

This brief has proposed the combination of single rail and dual rail encoding in register-less Null Convention Logic paradigm, which achieves low power consumption by eliminating pipeline registers, replacing complex completion detector with simpler OR gates, and mitigating the leakage power of sleepin blocks by fine-grain power gating. Compared with the register-less NCL, the RL-NCL implementation of the kogge-stone adder can reduce the power dissipation by 50% for the input data range 100MHz.

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