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Design of Fully Reused DSRC Encoders using SOLS Technique

Sreelakshmi K P[1], Baby Vineetha[2]
[1] *Mtech Student, MET'S School of Engineering, Mala, Thrissur, Kerala*
[2] *Professor, MET'S School of Engineering, Mala, Thrissur, Kerala*

Abstract: In the communication system the secure data transmission is very important. There are numbers of encoding techniques are used for the communication of data in DSRC. Several types of applications such as FM0, miller and Manchester encoding are used for the communication which provides the security to the data. The dedicated short-range communication (DSRC) system is the evolving technique used in the field of intelligent transport system (ITS) and Electronic Toll Collection (ETC). For obtaining DC balance, signal reliability, and to avoid noise interference DSRC adopts FMO, Manchester and Miller encoding. In this paper, Similarity Oriented Logic Simplification (SOLS) provides 100% Hardware Utilization Rate.

Keywords: FMO, Manchester, DSRC(Dedicated Short Range Communication),SOLS(Similarity Oriented Logic Simplification),ITS(Intelligent Transportation System), ETC(Electronic Toll Collection)

I. INTRODUCTION

Encoding technique is used in the communication system to convert the information of data into the suitable form of transmission. Encoding techniques are used for the purpose of security. There are different types of encoding techniques are used for the serial communication application. Several types of applications such as FM0, Manchester encoding, Miller encoding, NRZ, FM1, RZ, etc. are used for encoding of data in DSRC. The dedicated short-range communication (DSRC) is short range to medium range communication which can be communicated one or both ways in vehicle to vehicle (V2V) or vehicle to roadside (V2R) communications system. In vehicle -to- vehicle the DSRC equipment send and receives messages from one vehicle to other vehicle within the range. These messages include road safety instructions, traffic intimations; inter car distance, intersection warnings and collision alarms. The vehicle to roadside DSRC systems is mainly used for intelligent transport systems such as electronic toll collection, parking payments and gas refueling is used for encoding the data.

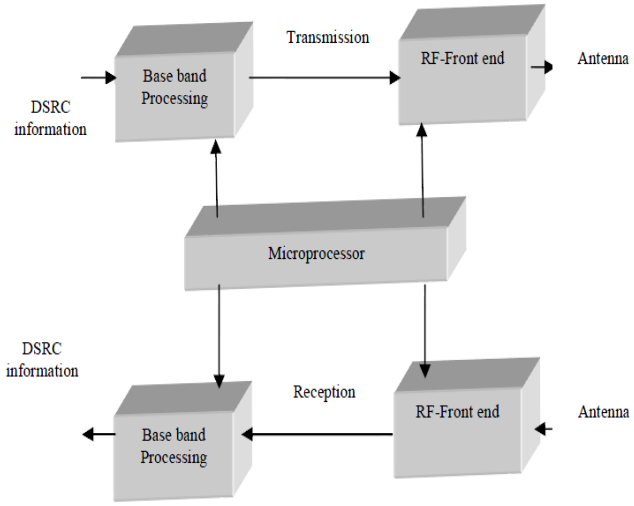

Figure 1: DSRC Transceiver

The architecture system of DSRC transceiver is as shown in Fig.1.The upper parts are dedicated for transmission and bottom parts are dedicated for receiving the information. The transceiver is classified into three modules: baseband processing, microprocessor, and RF front-end. The instructions of microprocessor interpret to schedule the tasks of baseband processing and RF front-end from media access control. The baseband processing is dependable for the error correction, modulation, and encoding and clock synchronization. The RF frontend transmits and receives the wireless signal through the antenna.

II. LITERATURE REVIEW

In [1], author proposed fully reused VLSI (Very Large Scale Integration) architecture by using SOLS technique for both the FM0 and Manchester encoding. The SOLS technique eliminates the limitations of hardware utilization by using two core techniques- (1) Area compact retiming and (2) Balance logic-operation sharing techniques. The Area compact retiming is used to reduce the hardware problem like number of transistor and the balance logic operation sharing the help identical logic components can be efficiently combines with the FM0 and Manchester encoding. In this paper the proposed method works on parameters like low power consumption, high operating frequency etc. This paper develops a fully reused VLSI architecture and also exhibits a competitive performance compared with the existing works. In [2]and [5], it is shown that an unbalance computation time results in the glitch at the input of MUX that causes the logic fault on coding. This paper overcomes the problem of glitches by using XNOR with the inverter by replacing the XOR and this becomes the input of the MUX.

This is done to balance the computational time. The adoption of FM0 or Manchester code depends on Mode and CLR signal. In this design both modes are separately allocated to system controller. Whether FM0 or Manchester code is adopted, all the logic component of the proposed VLSI architecture is utilized and provides better results. The work in [3] presents a review on Manchester, Miller and FM0 encoding techniques. This paper presents the circuit design strategies of Manchester, Miller and FM0 using a finite state machine. A comparative study of all these techniques is also presented in this work. [4] proposes a new Manchester code generator which behaves as an edge-triggered D flip-flop, except that the output is inverted on the clock falling edge .Operating frequencies up to 1 GHz can be expected in a standard 0.35 ~C MOS technology. In DSRC DC-Stability and signal reliability are fulfilled by FM0 and Manchester In [6] presents a review on evaluation of various forms of DSRC system. DSRC is the only short-range wireless alternative today that provides Fast Network Acquisition, Low Latency, High Reliability when Required, Priority for Safety Applications, Interoperability, Security and Privacy which is one of the challenging task faced by all in the worldwide.

In [7] proposed a fully reused VLSI architecture using the SOLS technique for both FM0 and Manchester encoding. The SOLS technique eliminates the limitation of hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The SOLS technique improves the hardware utilization rate from 57.14% to 100% for both FM0 and Manchester encodings. In [8] proposed a fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings. The coding diversity between FM0, Manchester and Miller encodings causes the limitation on hardware utilization of VLSI architecture design. In [9] proposed a system to minimize the problem of coding-diversity between FM0 and Manchester encodings that causes the limitation on hardware utilization of VLSI architecture design. In this paper, the fully reused VLSI architecture using SOLS technique for both FM0 and Manchester encodings is proposed. Area compact retiming and balance logic operation sharing are the two core techniques that are used to eliminate the limitation on hardware utilization by reducing the number of transistor and by combining the resources of FM0 and Manchester encodings.

III. PROPOSED ARCHITECTURE

In the proposed method we are introducing Miller encoding to the present structure. In the above papers, they are discussed about the fully reused architecture of FMO and Manchester Encoding using SOLS Technique.

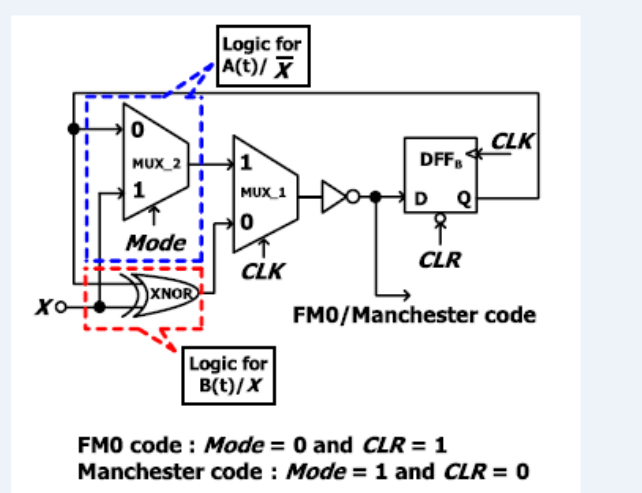

Figure 2: VLSI Architecture of FMO/ Manchester using SOLS Technique

The selection of FM0 or Manchester code depends on Mode and CLR signals. The CLR signal is used to reset all the contents. In addition, the CLR further has another individual function of a hardware initialization. If the CLR is simply derived by inverting Mode without assigning an individual CLR control signal, this leads to a conflict between the coding mode selection and the hardware initialization.

To avoid this conflict, both Mode and CLR are assumed to be separately allocated to this design from a system controller. Whether FM0 or Manchester code is adopted, no logic component of the proposed VLSI architecture is wasted. Every component is active in both FM0 and Manchester encodings while using the SOLS Technique. Miller encoding is also known as delay encoding. It can be used for higher operating frequency and it is similar to Manchester encoding except that the transition occurs in the middle of an interval when the bit is1. While using the Miller delay, noise interference can be reduced. Miller encoding is combined to FMO and Manchester encoding in order to avoid the complexity of the structure.

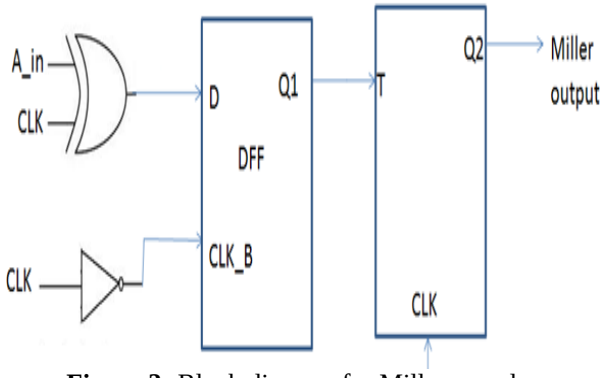

Figure 3: Block diagram for Miller encoder

The block diagram has a d flip flop, t flip flop, NOT gate, and XOR gate. Where the input is A_in and CLK, then the output is a Miller output. For example, if the input is 0 and the clock, given the XOR operation has done that, is A_in CLK , therefore 0 plus a positive edge clock produces the output as 0. Given to d flip flop, the clock has inverted, and after that output is given to t flip flop it inputs as d flip flop output, which is 0. Then the TFF is toggle FF, which produces the Miller output as 1.

In the proposed system, We have to effectively combines Miller encoding to the existing structure. Using SOLS Technique, we can share the same logic components between Miller and existing system. Both structures contain DFF and XOR. First divide the XNOR gate into XOR and inverter gate.

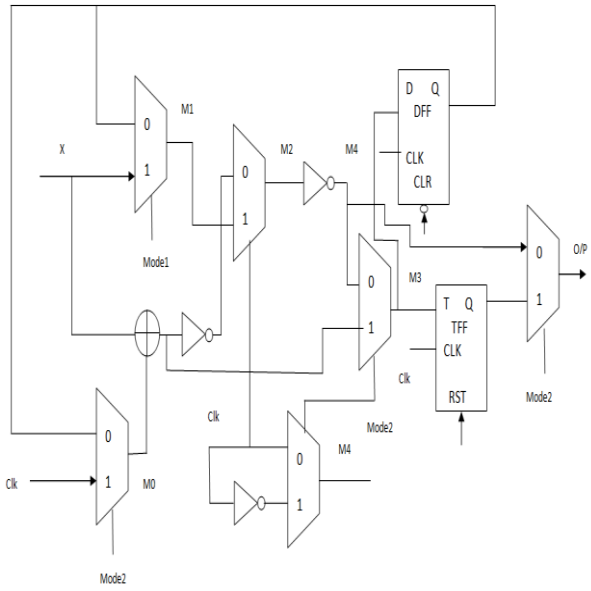

Figure 4: Fully Reused VLSI Architecture of FMO/ Manchester and Miller Encodings

In Fig. 4 Multiplexers are introduced to effectively combines both three encodings. Miller encoding needs negative clock. There are two mode signals are there one is mode1and mode2. If mode1 is active , it selects either FMO or Manchester according to the input signal X. If mode2 is active, Miller Encoding is

selected. CLR signal is present here to reset all the contents if Manchester encoding is selected. Without SOLS Technique, components used for the hardware architecture will be high. So power consumption of the structure, Area and delay will be high. SOLS Technique improves the Hardware Utilization Rate to 100%. The SOLS Technique classified into two techniques called Area compact retiming and Balance logic operation sharing to improve HUR and also to reduce Power, Area and Delay of the VLSI Architecture.

IV. RESULTS AND DISCUSSION

First modify the Hardware Architecture with Miller encoder without using SOLS Technique. SOLS technique includes Area compact retiming and Balance logic operation sharing. These two methods relocates hardware resources and sharing the same logic components between them. So the number of components will be high. It have poor Hardware Utilization Rate. Using SOLS Technique , Hardware utilization rate can be improved upto 100%. No even a single component is wasted. Then modify the fully reused structure of FMO and Manchester with Miller encoding using SOLS Technique.

Fig. 5 shows the simulation results without using SOLS Technique. Two mode signals are used here. The number of logic components are high. So this structure consumes more power. The number of logic components are high. It leads to increase in ciruit area and also increase the delay of the circuit. While using SOLS Technique, Reset signal is removed and CLR and MODE signals are used.

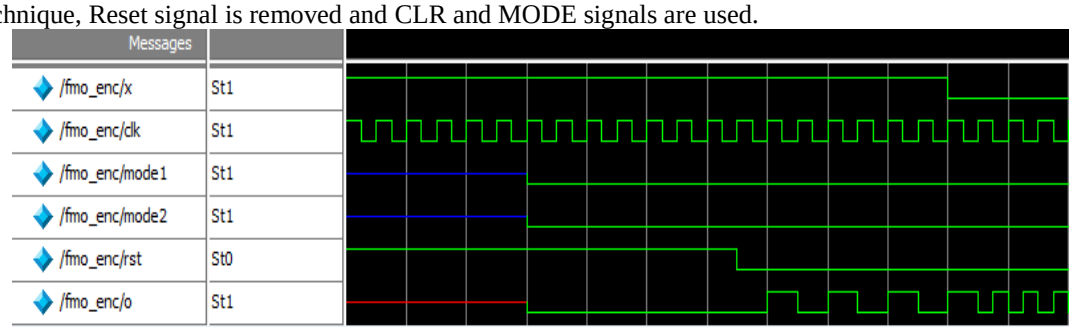

Figure 5: Simulation results without SOLS Technique

Fig.6 shows the simulation results using SOLS Technique. Three mode signals are used here. The simulation results in both cases are same.

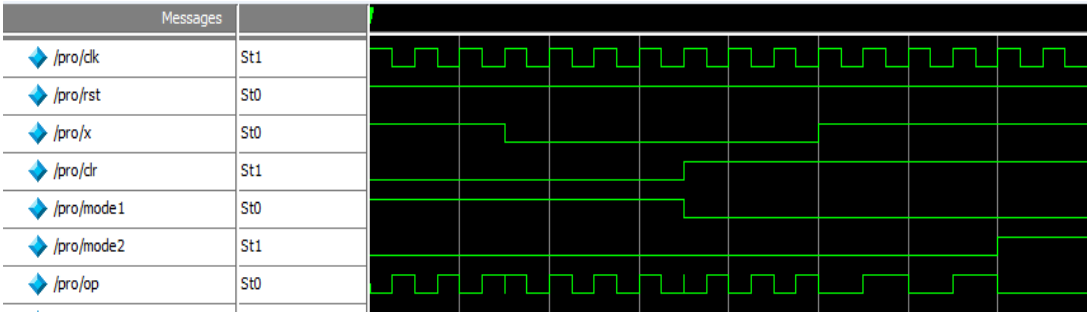

Figure 6: Simulation results using SOLS Technique

Xilinx tools are used to calculate the Power, Area and Delay in the above both cases. From the table, we can see that the reduction of power, area and delay of our proposed system while using SOLS Technique.

Table 1: Comparison Table of Power, Area and Delay

	Without SOLS Technique	With SOLS Technique
Power	672 mW	167mW
Area	70	61
Delay	11.839	9.59

V. CONCLUSION

In this paper, we have proposed a fully reused VLSI Architecture of FMO/ Manchester and Miller encoder using SOLS Technique for DSRC Applications. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic-operation sharing. The

area-compact retiming relocates the hardware resource to reduce the transistors. The balance logic-operation sharing efficiently combines FM0 and Manchester and Miller encodings with the identical logic components.

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