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Power Efficient PRPG using PRESTO Generator

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Abstract: Power, area and time are the major challenges for VLSI circuits. Power consumed during scan based test mode is much more than in normal mode because of increased switching transitions. This paper presents a low transition test pattern generator to reduce the power of a circuit during test by reducing the transitions within the random test pattern using PRESTO (preselected toggling) activity. LFSR is used as the PRPG. Bit Swapping Linear Feedback Shift Register (LFSR) is used to achieve power efficiency for Built-In-Self-Test (BIST) based VLSI architecture. BIST is a hardware entity and it has the ability of testing the circuit during manufacturing and also in situ conditions. Test pattern generations for VLSI testing fields demands low power designs, because the device dimensions are reducing drastically and most of them are made as portable devices (battery operated). Latest trends in test pattern generation consists of random pattern generator such as counter based circuits, scan chain based generators, LFSR in which LFSR is common. Bit Swapped LFSR based pattern generators are used to reduce transition power which is due to high switching activity in test vector generation. In this proposed design, a 25% reduction in power is attained.

Keywords: LFSR (Linear Feedback Shift Register), PRESTO (Preselected Toggling), BIST (Built in Self Test), VLSI (Very Large Scale Integration), DFT (Design for Testability)

I. INTRODUCTION

In future, the most crucial target of test assembling will stay same, basically to guarantee solid and high element semiconductor item conditions furthermore critical movement has been experienced by test arrangements. The design procedure, semiconductor technology and design characteristics are the key in components which will affect this development. Decade back test compression techniques were introduced, which has become quickly the core stream of Design for Test methodology. Power dissipation is a challenging problem for today's system-on-chips (SoCs) design and test. In general, power dissipation of a system in test mode is more than in normal mode. This is because a significant correlation exists between consecutive vectors applied during the circuit's normal mode of operation, whereas this may not be necessarily true for applied test vectors in the test mode. LBIST (logic-built-in-self-test) created for framework, board and test field is ahead of time for test generation as it will give exceptionally powerful Outline to Test and it has been used gradually more with test compression. Preserving all scan firmness and LBIST advantages, it can diminish the manufacturing cost of test. The variety of schemes used to decrease power through scan testing proposed.

There are various arrangements purposely projected for BIST, to maintain the peak power and average beneath given limit. For instance, the power used during test is decreased by preventing transitions at recollection elements. This will be generated by adding up gating logic in between logic driven by them and scan cell results. A burst clock controller backs off a portion of the movement cycles to diminish the voltage hang identified with a higher circuit action. It allows steady increase of circuit activity, in this manner decreasing di/dt effect. Depending upon the requirements for bit by bit warming of circuit shift clocks were gated by controller.BIST is an optimum solution for testing problems and provides maximum fault coverage.

It is a Design for Testability (DFT) methodology, which detects faulty components in a circuit by integrating test circuit on the chip itself. Testing is faster and efficient because testing circuit is built into hardware. BIST has many advantages such as at-speed testing and reduces the need of expensive Automatic test equipment.

Testing of internal modules and access to internal points is easy because of extra circuitry is built on the chip itself and testing can be done at normal operating speed. The cost of additional circuitry on chip is decreasing because of the betterment in the integration; hence BIST is a low cost test solution.

II. LITERATURE REVIEW

C Fagot et al proposed [2] a new effective Built-In Self Test (BIST) scheme that achieves 100% fault coverage with low area overhead, and without any modification of the circuit under test (CUT). The set of

patterns generated by a pseudo-random pattern generator, e.g. a Linear Feedback Shift Register (LFSR), is transformed into a new set of patterns that provides the desired fault coverage.

To transform these patterns, a ring architecture composed by a set of masks is used. During on-chip test pattern generation, each mask is successively selected to map the original pattern sequence into a new test sequence. We describe an efficient algorithm that constructs a ring of masks from the test cubes provided by an automatic test pattern generator (ATPG) tool. Moreover, we show that rings of masks are implemented very easily at low silicon area cost, without requiring any logic synthesis tool. Lakshmi Asokan et al proposed [3] a low power programmable pseudorandom pattern generator with desired toggling level and also enhanced fault coverage compared with other BIST based on PRPG. It comprised of finite state machine LFSR driving a phase shifter and it allows the device to produce binary sequence with preselected toggling activity. Generator is automatically controlled providing easy and precise tuning. Furthermore, this paper introduces a test compression method to avoid repeated pattern generation for testing the same device. The main highlight of this paper is to reduce the test data volume and test data memory. Bhunia proposes [4] new circuit so power dissipation during testing is reduced; this is obtained at input level of logic circuit by signal alteration masking. Addition of extra one transistor in logic circuit results advantages in the field of area, power and delay fields H. Mahmodi proposed [4] the implementation of masking effect by addition of supply gating in the path from supply to ground, at flip-flop output. E. G. McCluskey proposed [5] method fault coverage perfection for test per each scan, BIST is used for test circuit modification by adding test points or the redesigning of circuit is done. Bit fixing sequence generator architecture is designed by him, architecture is designed to change bits of pseudorandom sequence shifted to scan chain for the addition of test cubes into sequence [5].An easy way to comply with the paper formatting requirements is to use this document as a template and simply type your text into it.

M. Nourani et al proposes [6] a technique to detect a new test pattern generator for low- power BIST and scan-based BIST architectures. The proposed technique increases the correlation in two dimensions, i.e. vertical dimension between consecutive test patterns (Hamming Distance) and horizontal dimension between adjacent bits sent to a scan chain. Our technique reduces the primary inputs (PIs) activity of combinational circuits by increasing the correlation between consecutive patterns, i.e. transition between two consecutive patterns applied to CUT. It also reduces the switching activity in scan chain and its combinational clocks in a sequential circuit by reducing the transitions among adjacent bits in each pattern. Reducing the switching activity, in turn, results in reducing the power consumption, both peak and average.

III. EXISTING ARCHITECTURE

A. PRESTO Architecture:

The PRESTO Generator architecture with user defined inputs Switching code, Toggle code and Hold code is shown in Figure 1. Phase shifter will be connected to the PRPG by supplying scan chains, pseudorandom patterns are produced. The n numbers of hold latches are located between phase shifter and PRPG. Every hold latch is separately controlled by equivalent stage of n-bit control register.

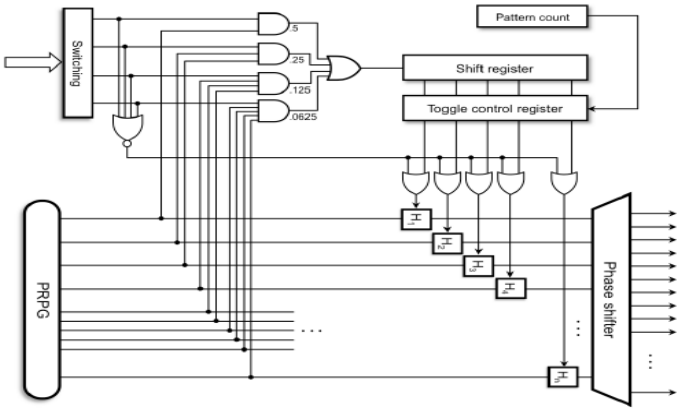

Figure 1: PRESTO Generator

When latch is enabled, data to the phase shifter will be given from the scan chains, if latches are disabled data to phase shifter will be given from PRPG.Loading the scan string with low transitions count patterns are not only allowed by PRESTO generator thus drastically reduces power dissipation, along with it enables the selections of its control such that generated test sequence consist of user distinct toggling rates. The

toggle control registers supervises hold latches which consists of 0s and 1s where 1s indicate toggle mode thus latch is transparent for data moving from PRPG. The toggle control register are loaded once per pattern count with additional shift register content and the enable signals for the shift register are produced in probalisitic manner by using original PRPG with programmable set of weights. The weights are determined by four AND gates producing 1s with probability 0.5, 0.25, 0.125, 0.0625 respectively. The OR gate allows choosing probabilities beyond powers of 2.

An additional 4-input NOR gate detects the switching code0000, which is used to switch the LP functionality off.So,while working in weighted random mode, the switching selector ensures stastically stable content of the control register in terms of amount of 1s it carries. Much higher flexibility in forming low-toggling test patterns can be achieved using this architecture. This approach splits up a shifting period of every test pattern into sequence of alternate toggle and hold intervals. To move to and forth between toggle and hold states, we use a T-flip flop that switches whenever there is at 1 on its data input. If it is set to 0, the generator enters in hold mode with temporarily disabling latches regardless of the toggle control register. If it is set to 1,it enables the latches and enters into toggle mode which moves data from PRPG to scan chains.

Two additional parameters kept in toggle and hold register determine how long the entire generator remains either in toggle or hold mode. To terminate either mode, a 1must occur on T-flip flop similar to that of a weighted logic used to feed the shift register. The T-flip flop controls four 2-input multiplexers routing data from toggle and control registers. It allows selecting a source of control data that will be used in the next cycle to change the operational mode of the generator test patterns. When using the PRESTO generator with existing DFT flow, all LP registers are either loaded once per test data registers or parts of an IJTAG network, and are initialized by the test setup procedure. Clearly, it suits LBIST applications where shift speeds are quite high.

B. Theoretical Calculation Of Toggling

Performance of the PRESTO generator depends primarily on the following three factors (note that in the BIST mode they are delivered only once, at the very beginning of the entire test session):

1. Switching Code.
2. Hold duty cycle.(HC)
3. Toggle duty cycle.(TC)

Given the size of PRPG, the number of scan chains and the corresponding phase shifter, the switching code as well as HC and TC values can be selected automatically in such a way that the entire generator will produce pseudorandom test patterns having a desired level of toggling T provided the scan chains are balanced. The procedure for selecting these parameters consists of many steps and values of switching, hold and toggle codes yields a ratio r with the smallest deviation from theoretical values using the equation,

$$A = (T \times S)/50 \qquad (1)$$

IV. PROPOSED ARCHITECTURE

In the proposed method, we are using Bit Swapping LFSR instead of conventional LFSR. Bit swapping LFSR (BS LFSR) is a modified version of conventional LFSR which generate pseudo random pattern at output of LFSR with less transition between 0 and 1, which occur in the LFSR output stream. It reduces the average power dissipated by CUT because of reduction in internal switching activity.

For the reduction of power, BS LFSR can be implemented either in Test-per-scan or Test-per-clock scheme. The power consumption of CUT mainly depends on the internal reduction of switching.

A. Bit Swapping LFSR

By reducing the number of transitions during test operation, BS LFSR reduces average and instantaneous, weighted switching activity. Power consumption can be reduced by several techniques. There are two direct techniques.

In the first direct technique, frequency is reduced during testing which in turn reduces power dissipation. This technique does not require extra hardware.

In the second direct technique, CUT is partitioned into blocks by applying appropriate test planning, to decrease power consumption. These direct techniques are not applicable for peak power reduction and also increase the test timing. BS LFSR reduces average and peak power dissipated by CUT, compared to other techniques. The basic Bit swapping LFSR is shown in Figure 2.Here; cn is taken as the selector line for the two multiplexers.

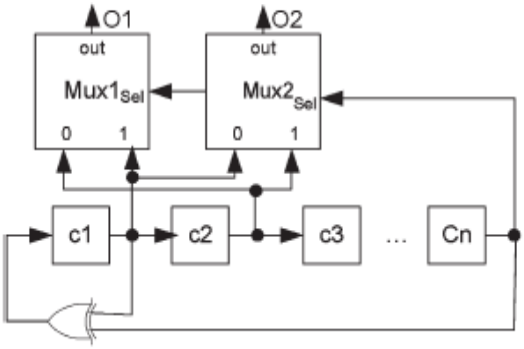

Figure 2: Bit Swapping LFSR

B. Bit Swapping Technique

Consider an n-bit maximal length LFSR. Let one of its outputs (last bit i.e. nth bit) to be a selection line that will swap two neighbouring bits. If the value of selection line is set to 0 for swapping and n is made odd (bit n=0), then bit 1 will be swapped with bit 2, bit 3 is swapped with bit 4…..bit n-2 with bit n-1. If n is made even (bit n=0), then bit will be swapped with bit 2, bit 3 with bit 4…bit n-3 with bit n-2. If n=1, then no swapping operation is performed. The number of transitions is saved by using swapping arrangement. Table 1 gives the transition count for LFSR with and without bit swapping.

Table 1: State Transition Chart for LFSR and Multiplexer

LFSR outputs of m, m+1									Multiplexers outputs O_1, O_2						
States			Next states			transition			states		Next States		transition		
c_1	c_2	c_n	c_1	c_2	c_n	c_1	c_2	∑	O_1	O_2	O_1	O_2	O_1	O_2	∑
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			0	0	1	0	0	0			0	0	0	0	0
0	0	1	1	0	0	1	0	1	0	0	0	1	0	1	1
			1	0	1	1	0	1			1	0	1	0	1
0	1	0	0	0	0	0	1	1	1	0	0	0	1	0	1
			0	0	1	0	1	1			0	0	1	0	1
0	1	1	1	0	0	1	1	2	0	1	0	1	0	0	0
			1	0	1	1	1	2			1	0	1	1	2
1	0	0	1	1	0	0	1	1	0	1	1	1	1	0	1
			1	1	1	0	1	1			1	1	1	0	1
1	0	1	0	1	0	1	1	2	1	0	1	0	0	0	0
			0	1	1	1	1	2			0	1	1	1	2
1	1	0	1	1	0	0	0	0	1	1	1	1	0	0	0
			1	1	1	0	0	0			1	1	0	0	0
1	1	1	0	1	0	1	0	1	1	1	1	0	0	1	1
			0	1	1	1	0	1			0	1	1	0	1
∑Transitions						**8**	**8**	**16**					**8**	**4**	**12**

In the above table without applying bit swapping the number of transitions in cell1 and cell2 are 8 and 8.But after applying bit swapping technique the number of transitions in same cell1 and cell2 are 8 and 4 respectively. So the total number of transitions is 16, without applying bit swapping and 12, after applying bit swapping technique. Hence the number of transitions are decreased implies power consumption is somehow decreased. Finally, the peak power is reduced by using this bit swapping technique. It is important to note that the overall savings of 25% is not equally distributed between the outputs of the multiplexers. This is because the value of c_1 in the present state will affect the value of c_2 and its own value in the next state (c_2 (Next) = c_1 and c_1 (Next) = c_1 xor c_n).

Let n=8. The number of transitions saved by swapping = T_{saved} = 26.

The number of transitions without swapping = 2x27= 28.

Therefore by swapping bits, T_{saved} = 26⁄28= 25% saved.

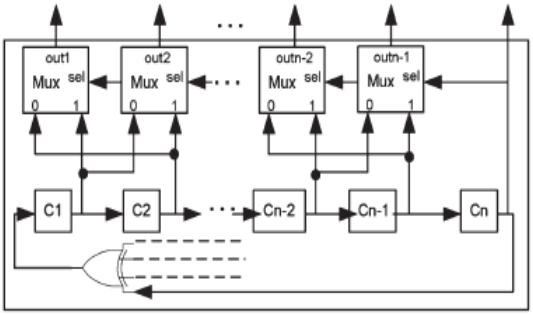

Figure 3: General Architecture of BS-LFSR

V. RESULTS AND DISCUSSION

A. Simulation Results

This section presents simulation results obtained for existing PRESTO generator and PRESTO with BS-LFSR.The generator primarily aims at reducing the switching activity during scan loading due to its preselected toggling levels and it allows loading the scan chains with patterns having low transitions. Simulation is done using 3 benchmark circuits. In this paper, simulation is done on Xilinx tool and ModelSim. Test pattern is generated using ModelSim and Power values are obtained from Xilinx. Table 2 gives the netlist for each benchmark circuit.

Table 2: Netlist for Benchmark Circuits

CIRCUIT	NETLIST
S27	4 inputs 1 output 3 D-type flip-flops 2 inverters 8 gates
S208	10 inputs 1 output 8 D-type flip-flops 38 inverters 66 gates
S298	3 inputs 6 outputs 14 D-type flip-flops 44 inverters 75 gates

These Benchmark circuits are taken from a set of ISCAS'89.ISCAS stands for International Symposium on Circuits and Systems. ISCAS mainly focuses on the significance of the circuits and systems fields, and also the growing technological applications and knowledge economy that is based on circuits and systems fundamentals. It is the annual conference of the IEEE Circuits and Systems Society, one of the oldest technical societies of IEEE with approximately 10,000 members worldwide. ISCAS welcomes technical contributions and participation from all researchers and practitioners in the field of circuits and systems. ModelSim outputs are given below:

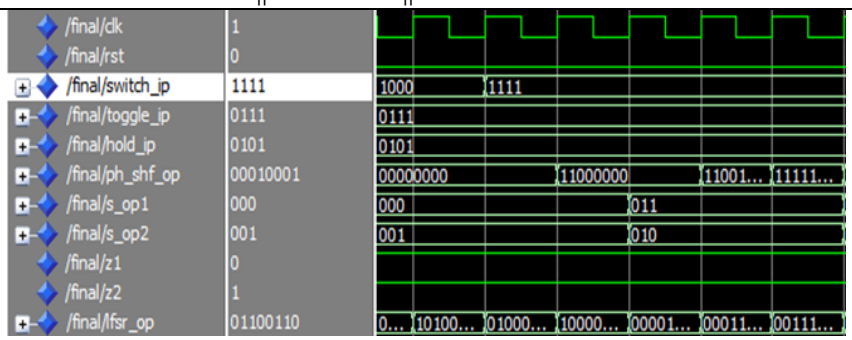

Figure 4: S27 Existing Output

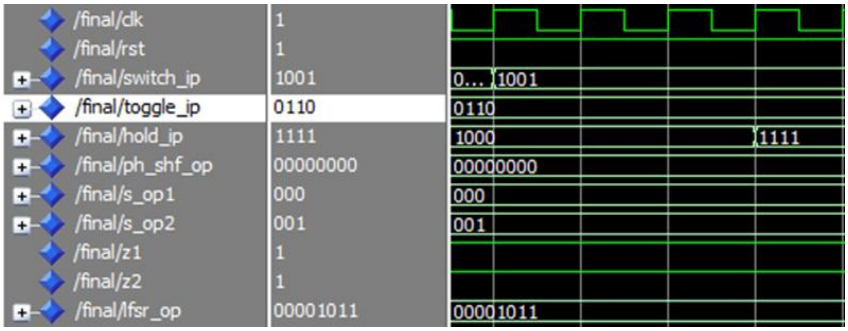

Figure 5: S27 Proposed Output

Power consumption values are measured for each circuit. They are listed below:

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		130
Vccint 1.80V:	69	123
Vcco33 3.30V:	2	7
Clocks:	45	81
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0

Figure 6: S27 Existing Output

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		123
Vccint 1.80V:	64	116
Vcco33 3.30V:	2	7
Clocks:	41	74
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0

Figure 7: S27 Proposed Output

Figure 6 and Figure 7 show the Xilinx power analysis for the benchmark circuit S27.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		145
Vccint 1.80V:	77	138
Vcco33 3.30V:	2	7
Clocks:	53	96
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Figure 8: S208 Existing Output

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		126
Vccint 1.80V:	67	120
Vcco33 3.30V:	2	7
Clocks:	43	78
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Figure 9: S208 Proposed Output

Figure 8 and Figure 9 show the Xilinx power analysis for the benchmark circuit S208.

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		159
Vccint 1.80V:	84	152
Vcco33 3.30V:	2	7
Clocks:	61	110
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

Figure 10: S298 Existing Output

Power summary:	I(mA)	P(mW)
Total estimated power consumption:		149
Vccint 1.80V:	79	142
Vcco33 3.30V:	2	7
Clocks:	55	100
Inputs:	8	15
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	15	27
Quiescent Vcco33 3.30V:	2	7

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Figure 11: S298 Proposed Output

Figure 10 and Figure 11 show the Xilinx power analysis for the benchmark circuit S298.The table below gives the compared values between existing and proposed.

Table 3: Power Comparison Table

BENCHMARK CIRCUIT	POWER (mW)
S27 existing	130
S27 proposed	123
S208 existing	145
S208 proposed	126
S298 existing	159
S298 proposed	149

VI. CONCLUSIONS

In this paper, we have proposed a Test pattern generation method, where patterns are generated using PRPG. The PRESTO configuration generates pattern with preselected toggling rate, i.e. the pattern produced will have user distinct toggling rate. So the switching activity of sequence will be reduced due to preselected toggling and thereby power utilization is reduced. PRESTO is modified with a Bit Swapping LFSR. When BS-LFSR is used, power can be substantially reduced. Comparisons between the proposed design and other previously published methods show that the proposed design can achieve better results for most tested benchmark circuits.

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